CLAIMS

[1] A semiconductor device comprising a silicon substrate, a gate insulating film formed on said silicon substrate, and a gate electrode formed on said gate insulating film,

characterized in that said gate insulating film includes an electrically insulating film having a high dielectric constant and containing one of metal oxide, metal silicate and metal oxide or metal silicate containing nitrogen therein,

said gate electrode has a region through which said gate electrode makes contact with said gate insulating film and which contains silicide of metal M as a primary constituent, said silicide being expressed with $MxSi_{1-X}$ ($0<X<1$), and

said X is greater than 0.5 ($X>0.5$) in said silicide of metal M contained in a gate electrode formed above a p-channel, and said X is equal to or smaller than 0.5 ($X\leq0.5$) in said silicide of metal M contained in a gate electrode formed above a n-channel.

[2] The semiconductor device as set forth in claim 1, wherein said electrically insulating film contains one of Hf and Zr.

[3] The semiconductor device as set forth in claim 1, further comprising a layer containing one of Hf and Zr therein between said electrically insulating film and said gate electrode.

[4] The semiconductor device as set forth in claim 1, wherein said electrically insulating film has a multi-layered structure including one of a silicon oxide film and a silicon nitride film, and one of a Hf-containing layer and a Zr-containing layer.

[5] The semiconductor device as set forth in claim 1, wherein said electrically insulating film contains HfSiON.

[6] The semiconductor device as set forth in claim 1, further comprising a HfSiON layer between said electrically insulating film and said gate electrode.

[7] The semiconductor device as set forth in claim 1, wherein said electrically insulating film has a multi-layered structure including one of a silicon oxide film and a silicon nitride film, and a HfSiON layer.

[8] The semiconductor device as set forth in any one of claims 1 to 7, wherein said metal M is a metal to which a salicide process is applicable to make silicide.

[9] The semiconductor device as set forth in any one of claims 1 to 7, wherein said metal M is nickel (Ni).

[10] The semiconductor device as set forth in claim 9, wherein, assuming that a region of said silicide (including nickel (Ni) as said metal M) making contact with said gate insulating film is expressed with Ni_XSi_{1-X} ($0<X<1$), said X is equal to or greater than 0.6 and smaller than 1 ($0.6 \leq X<1$) in said silicide contained in a gate electrode formed above a p-channel, and said X is greater than 0 and equal to or smaller than 0.5 ($0<X \leq 0.5$) in said silicide contained in a gate electrode formed above a n-channel.

[11] The semiconductor device as set forth in claim 9, wherein said silicide contained in said gate electrode formed above said p-channel contains Ni_3Si phase as a principal constituent at least in a region through which said silicide makes contact with said gate insulating film, and said silicide contained in said

gate electrode formed above said n-channel contains one of NiSi phase and $NiSi_2$ phase as a principal constituent at least in a region through which said silicide makes contact with said gate insulating film.

[12] A semiconductor device comprising a silicon substrate, a gate insulating film formed on said silicon substrate, and a gate electrode formed on said gate insulating film,

characterized in that at least a region of said gate electrode making contact with said gate insulating film is composed of silicide containing Ni_3Si phase as a principal constituent.

[13] The semiconductor device as set forth in claim 12, wherein said gate insulating film includes an electrically insulating film having a high dielectric constant and containing one of metal oxide, metal silicate and metal oxide or metal silicate containing nitrogen therein,

[14] The semiconductor device as set forth in claim 13, wherein said electrically insulating film contains one of Hf and Zr.

[15] The semiconductor device as set forth in claim 13, further comprising a layer containing one of Hf and Zr therein between said electrically insulating film and said gate electrode.

[16] The semiconductor device as set forth in claim 13, wherein said electrically insulating film has a multi-layered structure including one of a silicon oxide film and a silicon nitride film, and one of a Hf-containing layer and a Zr-containing layer.

[17] The semiconductor device as set forth in claim 13, wherein said

electrically insulating film contains HfSiON.

[18] The semiconductor device as set forth in claim 13, further comprising a HfSiON layer between said electrically insulating film and said gate electrode.

[19] The semiconductor device as set forth in claim 13, wherein said electrically insulating film has a multi-layered structure including one of a silicon oxide film and a silicon nitride film, and a HfSiON layer.

[20] The semiconductor device as set forth in any one of claims 12 to 19, wherein said gate electrode is included in a p-type MOSFET.

[21] A method of fabricating a semiconductor device defined in any one of claims 1 to 9, comprising:

depositing poly-silicon (poly-Si) on a gate insulating film and patterning said poly-silicon into a gate electrode having desired dimension;

depositing metal M on said gate electrode;

thermally annealing said gate electrode and said metal M to entirely turn said gate electrode to silicide of said metal M; and

removing a portion of said metal M which was not turned into said silicide, by etching,

wherein said metal M has such a thickness t1 above a p-channel device that, when poly-silicon and said metal M react with each other to make silicide, a portion of said silicide making contact with said gate insulating film has composition expressed with $MxSi_{1-X}$ ($0.5<X<1$), and has such a thickness t2 above a n-channel device that, when poly-silicon and said metal M react with each other to make silicide, a portion of said silicide making contact with said gate insulating film has composition expressed with $MxSi_{1-X}$ ($0<X\leq0.5$).

[22] A method of fabricating a semiconductor device defined in claim 10, comprising:

depositing poly-silicon on a gate insulating film and patterning said poly-silicon into a gate electrode having desired dimension;

forming a nickel (Ni) film on said gate electrode;

thermally annealing said gate electrode and said nickel film to entirely turn said gate electrode to nickel silicide (NiSi); and

removing a portion of said nickel film which was not turned into said nickel silicide, by etching,

wherein said nickel film has such a thickness t1 above a p-channel device that, when poly-silicon and nickel react with each other to make nickel silicide, a portion of said nickel silicide making contact with said gate insulating film has composition expressed with Ni_XSi_{1-X} ($0.6 \leq X < 1$), and has such a thickness t2 above a n-channel device that, when poly-silicon and nickel react with each other to make nickel silicide, a portion of said nickel silicide making contact with said gate insulating film has composition expressed with Ni_XSi_{1-X} ($0 < X \leq 0.5$).

[23] A method of fabricating a semiconductor device defined in claim 11, comprising:

depositing poly-silicon on a gate insulating film and patterning said poly-silicon into a gate electrode having desired dimension;

forming a nickel (Ni) film on said gate electrode;

thermally annealing said gate electrode and said nickel film to entirely turn said gate electrode to nickel silicide (NiSi); and

removing a portion of said nickel film which was not turned into said nickel silicide, by etching,

wherein said nickel film has such a thickness t1 above a p-channel device that, when poly-silicon and nickel react with each other to make nickel silicide, said nickel silicide has Ni_3Si phase as a principal constituent, and has such a

thickness t2 above a n-channel device that, when poly-silicon and nickel react with each other to make nickel silicide, said nickel silicide has one of NiSi phase and $NiSi_2$ phase as a principal constituent.

[24] The method as set forth in claim 23, wherein a ratio of a thickness TNi of said nickel film to a thickness TSi of said poly-silicon is defined as $TNi/TSi \geq 1.60$ to form said gate electrode including Ni_3Si phase as a principal constituent.

[25] The method as set forth in claim 23, wherein a ratio of a thickness TNi of said nickel film to a thickness TSi of said poly-silicon is defined as $0.55 \leq TNi/TSi \leq 0.95$ to form said gate electrode including NiSi phase as a principal constituent.

[26] The method as set forth in claim 23, wherein a ratio of a thickness TNi of said nickel film to a thickness TSi of said poly-silicon is defined as $0.28 \leq TNi/TSi \leq 0.54$, and said gate electrode and said nickel film are thermally annealed at 650 degrees centigrade or higher to form said gate electrode including $NiSi_2$ phase as a principal constituent.

[27] The method as set forth in any one of claims 21 to 23, wherein the step of depositing said metal M or forming said nickel film comprises:

after forming said metal M or said nickel film above a n-channel device or a p-channel device by the thickness of t2, forming diffusion-preventing layer which is stable to said metal M or nickel, only above said n-channel device; and

depositing said metal M or forming said nickel film by the thickness of (t1 - t2).

[28] The method as set forth in claim 27, wherein said diffusion-preventing layer can be etched in selected areas relative to silicide of said metal M.

[29] The method as set forth in claim 27, wherein said diffusion-preventing layer contains one of TiN and TaN as a primary constituent.

[30] The method as set forth in any one of claims 21 to 29, wherein said gate electrode and said metal M or said nickel film are thermally annealed for silicidation at such a temperature that a resistance of metal silicide formed in a diffusion contact region of said semiconductor device is not increased.

[31] A method of fabricating a semiconductor device defined in claim 10, comprising:

depositing poly-silicon on a gate insulating film and patterning said poly-silicon into a gate electrode having desired dimension;

forming a nickel (Ni) film on said gate electrode;

thermally annealing said gate electrode and said nickel film to entirely turn said gate electrode to nickel silicide (NiSi); and

removing a portion of said nickel film which was not turned into said nickel silicide, by etching,

wherein a ratio of a thickness TNi of said nickel film to a thickness TSi of said poly-silicon is defined as $1.60 \leq TNi/TSi$.